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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,426	08/30/2001	Vladislav Vashchenko	75292/13356	1844

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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10/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/944,426	VASHCHENKO, VLADISLAV	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of forming at least one additional p+ region and at least one n+ region inside the p-well of the structure to define at least **one p-n junction** between the p-type material as defined by the p-well and one of the additional p+ regions in the p-well on the one hand, and the n-type material of one of the additional n+ regions in the p-well on the other hand, as recited in claim 2, are unclear as to which junction is the one p-n junction, because applicant recites forming the p-n junction between the p-type material of the p-well and one of the additional p+ regions and the n-type material of one of the additional n+ regions. Note that one p-n junction is formed only between two materials.

The claimed limitations of “the additional p+ regions” and “the additional n+ regions”, as recited in claim 2, are unclear as to which elements are the “the additional p+ regions” and “the additional n+ regions”, and the structural relationship between the “the additional p+ regions” and “the additional n+ regions” and the LVTSCR structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (6,573,566) in view of Yu (5,361,185).

Regarding claim 2, Ker et al. teach in figure 8B and related text a method of increasing the holding voltage of an LVTSCR structure that includes an n-well 208 and a p-well 206 formed in a substrate 200, a first n+ region 214 and a first p+ region 212 formed in the n-well to define a high voltage node,

the method comprising: forming at least one additional p+ region 222 and at least one n+ region 220 inside the p-well of the structure to define at least one p-n junction between the p-type material as defined by the p-well and one of the additional p+ regions in the p-well on the one hand, and the n-type material of one of the additional n+ regions in the p-well on the other hand,

the p-n junction being forward biased during normal operation by having said additional p+ region of the p-n junction located closer to the high voltage node than the additional n+ region of the p-n junction.

Regarding claims 3-4, Ker et al. teach in figure 8B and related text a method of increasing the holding voltage of an LVTSCR structure having an anode in an n-well and a cathode in a p- well, comprising

forming at least one additional n+ region 220 and at least one additional p+ region 222 in the p-well to define at least one forward biased diode under normal operation in the p-well, thereby providing an alternative current path from anode to cathode through said at least one diode,

wherein the alternative current path defines a lower resistance current path than the p-well.

Ker et al. do not teach in the embodiment of figure 8B and a second n+ region and a second p+ region formed in the p-well.

Ker et al. teach in figure 10B a diode 324 connected to the cathode of SCR G2.

Yu teaches in figure 4 and related text a diode comprising an n+ region 50 and a p+ region 56 formed in a p substrate 24.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a diode comprising an n+ region and a p+ region in the p-well in Ker et al.'s device in order to provide protection to the device, and in order to reduce the size of the device and to simplify the processing steps of making the device.

Response to Arguments

Applicant argues that the claimed limitations of "the additional p+ regions" and "the additional n+ regions", as recited in claim 2, are clear.

The claimed limitations of "the additional p+ regions" and "the additional n+ regions", as recited in claim 2, are unclear because applicant claims only one "additional p+ region" and one "additional n+ region", and the structural relationship between the "the additional p+ regions" and "the additional n+ regions" and the LVTSCR structure is unclear.

Applicant argues that the claimed limitations of forming at least one additional p+ region and at least one n+ region inside the p-well of the structure to define at least **one p-n junction** between the p-type material of the p-well and one of the additional p+ regions in the p-well on the one hand, and the n-type material of one of the additional n+ regions in the p-well on the other hand, as recited in claim 2, are clear because "the n-material is defined by an additional n+ region and two p-doped material of different doping density as defined by the p-well, and a highly doped region defined by the additional p+ region which forms the anode of the diode. Hence, both the low doped p-well and the highly doped additional p+ region are included in the recitation of the diode structure".

Although applicant acknowledges that one p-n junction is formed only between two materials, applicant still states that more than two materials/elements are involved

in said one p-n junction. Therefore, it is unclear how a junction, which is the boundary between two elements can comprise more than two elements.

Applicant argues that Ker et al. do not teach a method of increasing the holding voltage of an LVTSCR structure.

The claimed limitation of a method of increasing the holding voltage of an LVTSCR structure is inherent in Ker et al.'s device for the following reasons. The claimed structure is identical to prior art's structure. Since the claimed structure increases the holding voltage of the LVTSCR structure, then prior art's structure also increases the holding voltage of the LVTSCR structure.

Furthermore, the recitation of increasing the holding voltage of an LVTSCR structure has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Applicant argues that Ker et al. do not teach at least one additional p+ region and at least one n+ region inside the p-well, because said regions define the cathode.

Claim 2 recites "at least one additional p+ region and at least one n+ region inside the p-well". Ker et al. teach one p+ region and at least one n+ region inside the p-well. Therefore, Ker et al. teach at least one additional p+ region 222 and at least one n+ region 220 inside the p-well, as claimed.

Applicant argues that Ker et al. teach external diode, whereas the present invention seeks to avoid the inclusion of external diodes.

The examiner does not suggest the inclusion of external diodes. The examiner states that Ker et al. teach in figure 10B a diode 324 connected to the cathode of SCR G2 in order to provide motivation for an artisan to form a diode in the device of the embodiment of figure 8B of Ker et al.

Applicant argues that there is no suggestion in prior art to include diodes to avoid the latch-up problems of an LVTSCR, as disclosed by the present invention.

In response to applicant's argument that there is no suggestion in prior art to include diodes to avoid the latch-up problems of an LVTSCR, as disclosed by the present invention, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
11/1/2008

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TECHNOLOGY CENTER 2800